

SYSTEMS, PROCESSES AND INTEGRATED CIRCUITS
FOR IMPROVED PACKET SCHEDULING OF MEDIA OVER PACKET

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ABSTRACT:

One method of processing first and second received packets of real-time information includes computing for each of said received packets respective deadline intervals and ordering processing of the first and second received packets according to the respective deadline intervals. A single-chip integrated circuit has a processor circuit and embedded electronic instructions forming an egress packet control establishing an egress scheduling list structure and operations in the processor circuit that extract a packet deadline intervals DI, place packets in the egress scheduling list according to deadline intervals DI; and embed a decoder that decodes the packets according to a priority depending to their deadline intervals. Embedded electronic instructions establish an egress scheduling list structure and operations in the processor circuit that establish channel decoders on non-coincident frame boundaries and a packet engine to detect when a first packet has a first deadline and is currently in decode while a second packet is just-arriving and has a second deadline earlier than the first deadline. The packet engine establishes a determination whether both the second and first packets can be decoded ahead of their respective deadlines if the second packet were decoded preemptively, and if so, then preempts the processor circuit channel decoder structure to decode the second packet. Other processes, integrated circuits, chipsets, wireless telephones, PBXs, line

